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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,686	08/24/2001	Masahiro Kamiya	11-055	3386

23400 7590 06/10/2004

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EXAMINER	
VO, TED T	
ART UNIT	**PAPER NUMBER**
2122	

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,686	KAMIYA ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/24/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed on 08/24/2001.

Claims 1-9 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Mitsuishi (US Pat. No. 6,745,320 B1).

Given the broadest reasonable interpretation of followed claims in light of the specification:

As per claim 1: Mitsuishi discloses,

A compiler for processing computer program source code, to generate object code to be executed by a RISC (Reduced Instruction Set Computer) type of CPU (central processing unit) of a

computer (See FIG. 42, or column 68, lines 21-42; and see column 5, lines 52-67, "an application field mainly using programming by high-level language"), *said object code including code for an instruction for judging the value of a bit variable and an instruction for assigning a value to a bit variable* (See "bit test instruction", FIGs. 54, 75, 76), *said bit variables being held in a memory or a register of said computer* (FIG. 54), *wherein*

said object code is generated such that, when said object code is executed, processing is performed whereby a bit operational expression which is written within said source code is converted to a condition judgement expression which judges the respective values of bit variables that are operands of said bit operational expression (the use of bit test instruction and bit set instruction at register level such as it is shown in FIGs 75-77), *and whereby a predetermined first binary value and a predetermined second binary value are selectively assigned to a bit variable which holds a result of said bit operational expression, in accordance with whether a "true" or a "false" decision is obtained from said condition judgement expression* (The execution of bit test instruction causes a flag is set. For example, "The bit test instruction inspects predetermined bits of data on the general purpose register or on the address space and reflects the inspection result to Z flag of CCR" (column 78, lines 51-55). The bit test instruction results a branch decision based on true or false (see column 80, lines 5-21)).

As per Claim 2: Mitsuishi discloses,

The compiler according to claim 1, wherein a set of bit variables held in an internal register of said CPU can be processed as a register variable, and wherein said condition judgement expression judges the values of respective ones of said set of bit variables. (See column 78, lines 51-55, "The bit test instruction inspects predetermined bits of data on the general purpose register or on the address space and reflects the inspection result to Z flag of CCR").

As per Claim 3: Mitsuishi discloses, *A data storage medium having a compiler as claimed in claim 1 stored therein.* (See FIG. 42).

As per Claim 4: Regarding, "*A program conversion apparatus for reading out the contents of a source code file which is stored as a program, and for converting said source code file to an object code file whose contents are to be executed by a RISC (Reduced Instruction Set Computer) type of CPU (central*

processing unit) of a computer, said object code including an instruction for judging the value of a bit variable and an instruction for assigning a value to a bit variable, said bit variables being held in a memory or a register of said computer, wherein said program conversion apparatus comprises memory means having stored therein a compiler for generating object code such that, when said object code is executed, processing is performed whereby a bit operational expression which is written within said source code is converted to a condition judgement expression which judges the respective values of bit variables that are operands of said bit operational expression, and whereby a predetermined first binary value and a predetermined second binary value are selectively assigned to a bit variable which holds a result of said bit operational expression, in accordance with whether a "true" or a "false" decision is obtained from said condition judgement expression": The limitation has the functionality corresponding to the limitation of Claim 1. See Rationale of Claim 1 above.

As per Claim 5: Regarding, "*The program conversion apparatus according to claim 4, wherein said compiler is capable of generating object code whereby a set of bit variables held in an internal register of said CPU are processed as a register variable, and wherein and wherein said condition judgement expression judges the values of respective ones of said set of bit variables*": The limitation has the functionality corresponding to the limitation of Claim 2. See Rationale of Claim 2 above.

As per Claim 6: Claim 6 has the limitation corresponding to the functionality of Claim 1. See Rationale of Claim 1 above.

As per Claim 7: Claim 7 has the limitation corresponding to the functionality of Claim 2. See Rationale of Claim 2 above.

As per Claim 8: Claim 8 has the limitation corresponding to the functionality of Claim 1. See Rationale of Claim 1 above.

As per Claim 9: Claim 9 has the limitation corresponding to the functionality of Claim 2. See Rationale of Claim 2 above.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

UTMC Microelectronic Systems Inc., "UT1750AR RISC Assembly Language Manual", 1998, discloses bit operations in RISC architecture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552.

The fax phone numbers:

(703) 872-9306 (for formal communication intended for entry);

(703) 746-5429 (for informal or draft communication, please label "PROPOSED" or "DRAFT").

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TED T. VO

Patent Examiner
Art Unit: 2122
June 04, 2004